Description

[ACCESS METHOD FOR EMBEDDED JTAG TAP CONTROLLER INSTRUCTION REGISTERS]

BACKGROUND OF INVENTION

[0001] The present invention generally relates to an integrated circuit chip structure that has a chip level test access port (TAP) controller and more particularly to a chip that also includes a plurality of embedded TAPs connected to the chip level TAP. Because the embedded TAPs have instruction register (IR) lengths that differ from the chip level TAP IR, and the embedded TAP IR lengths may differ from each other, the chip level TAP includes a flexible length instruction register architecture designed to accommodate the different length instruction registers of the embedded TAPs while using a constant length chip level instruction register definition for all IR accesses through the chip level TAP.

[0002] As explained in U.S. Patent 6,334,198 (incorporated

herein as reference) the electronics industry continues to rely upon advances in semiconductor technology to realize higher-functioning devices in more compact areas. For many applications, realizing higher-functioning devices requires integrating a large number of electronic devices into a single silicon wafer. As the number of electronic devices per given area of the silicon wafer increases, the manufacturing process becomes more difficult.

[0003] A wide variety of techniques have been used in IC devices to ensure that, once they are manufactured, they operate fully in compliance with their intended design and implementation specifications. Many of the more complex IC designs include circuits that permit in-circuit testing via the IC access pins. The IEEE 1149.1 JTAG recommendation, for example, provides a test circuit architecture for use inside such ICs. This architecture includes a test access port (TAP) controller coupled to the IC pins for providing access to and for controlling various standard features designed into such ICs. Some of these features are internal scan, boundary scan, built-in test, and emulation.

[0004] The JTAG recommendation was developed with the understanding that such IC designs would be using only one TAP controller. Sometime after the TAPs, initial develop-

ment, however, many IC's were designed with multiple "core" circuits, such as multiple CPUs, with each core circuit including its own TAP controller. Typically, separate IC pins are used to select one of the TAP controllers for testing and/or debugging the IC. This is problematic, however, in IC applications that require an increasing number of core circuits without increasing the circuit area of the IC and/or the number of IC pins.

[0005] ASIC (application specific integrated circuit) devices, usually contain a single JTAG TAP controller for access and control of board level tests of I/O continuity. Access to user defined functions can also be supported using the chip level TAP controller and private instruction definitions. When integrating large intellectual property (IP) blocks into today's ASICs there is the possibility that such IP will have embedded JTAG access through a self contained TAP controller. Access methods for embedded TAP functions are not covered in the IEEE1149.1 JTAG specification. Methods have evolved, independent of the IEEE1149.1 specification, that enable access to embedded TAP controllers through the use of various implementations of compliance enable logic and private instruction definitions in the ASICs chip level TAP controller. These

methods strive to maintain IEEE1149.1 JTAG compliance; however, one limitation of these existing methods is the inability to shift out (or read) differing length embedded TAP instruction registers with a single chip level instruction register length definition as is required for IEEE1149.1 compliance.

[0006] This invention described below allows IEEE1149.1 compliant shifting out (reading) of embedded JTAG TAP controller instruction register (IR) contents, contained in IP blocks on ASIC chips, while using a constant length chip level instruction register definition for all IR accesses through the chip level TAP .

SUMMARY OF INVENTION

[0007] This disclosure presents an integrated circuit chip structure that has a chip level test access port (TAP) controller and a plurality of embedded TAPs connected to the chip level TAP. Because the embedded TAPs have instruction register lengths that differ from the chip level TAP IR, and the embedded TAP IR lengths may differ from each other, the chip level TAP includes a flexible length instruction register architecture designed to accommodate the different length instruction registers of the embedded TAPs, while using a constant length chip level instruction regis-

ter definition for all IR accesses through the chip level TAP. Further, the invention includes selection logic adapted to actively connect only a single embedded TAP to the chip level TAP at a time.

[0008] This chip-level flexible length instruction register length is longer than the longest embedded TAP instruction register, and the additional bits that make the flexible length instruction register longer than the longest embedded TAP instruction register comprises bits that are adapted to choose the active length of the flexible length instruction register.

[0009] The inventive flexible length instruction register comprises of several segments of register bits, including a plurality of multiplexers used to selectively concatenate or bypass the register segments with the selected embedded TAP instruction register bits, maintaining a constant length chip-level TAP instruction register. The length of the register segments are, for example in one embodiment, a first instruction register segment having the same length as the shortest embedded TAP instruction register, and a second instruction register segment having a length equal to the difference between the shortest embedded TAP instruction register and a larger embedded TAP in-

struction register. More generally, the flexible length instruction register comprises additional instruction registers segments having incremental lengths equal to the difference between the previous shorter embedded TAP instruction register and the next largest embedded TAP instruction register.

[0010] The invention includes a plurality of multiplexors connected to the additional instruction registers segments, wherein the multiplexors are adapted to selectively include incremental ones of the additional instruction registers segments to incrementally match the difference in length of longer embedded TAP instruction registers and the chip-level TAP instruction register. Thus, the active length of the flexible length instruction register comprises the selected embedded TAP instruction register bits combined with selected ones of the additional instruction registers segments of the chip-level TAP instruction register.

[0011] One benefit of the invention is that the flexible length instruction register appears as a fixed length instruction register to users connecting to the chip level TAP. Therefore , the invention allows IEEE1149.1 compliant access (reading) of embedded JTAG TAP controller instruction register (IR) contents, contained in IP blocks on ASIC

chips, while using a constant length chip level instruction register definition for all IR accesses through the chip level TAP. More specifically, the invention allows positional bit replacement of the chip level TAP IR data with embedded TAP IR data. The new architecture allows for a single IR length definition to represent and access all embedded and chip level TAP instruction registers.

[0012]   These, and other, aspects and objects of the present invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the present invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the present invention without departing from the spirit thereof, and the invention includes all such modifications.

BRIEF DESCRIPTION OF DRAWINGS

[0013]   The invention will be better understood from the following detailed description with reference to the drawings, in which:

[0014]   Figure 1 is a conceptual diagram of the chip level and em-

bedded TAPs used with the inventive structure:

[0015] Figure 2 is a schematic diagram of different length instruction registers included within the chip level and embedded TAPs;

[0016] Figure 3 is a schematic diagram of the chip level and embedded TAPs used with the inventive structure; and

[0017] Figure 4 is a schematic diagram of the chip level and embedded TAPs used with the inventive structure.

DETAILED DESCRIPTION

[0018] The present invention and the various features and advantageous details thereof are explained more fully with reference to the non-limiting embodiments that are illustrated in the accompanying drawings and detailed in the following description. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the present invention. The examples used herein are intended merely to facilitate an understanding of ways in which the invention may be practiced and to further enable those of skill in the art to practice the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

[0019] Figure 1 illustrates a first embodiment of the inventive integrated circuit chip structure. As shown in Figure 1, the chip 100 (which can be, for example an ASIC) includes a chip level test access port (TAP) controller 102 and a plurality of embedded TAPs 104-110 connected to the chip level TAP. A user 150 will access the data within the embedded TAPs 104-110 through the chip level TAP controller 102. Note that the length of the instruction registers 112-118 within each of the embedded TAPs is inconsistent. For example, instruction register 112 is four bits long, instruction registers 114 and 116 are six bits long, and instruction register 118 is ten bits long.

[0020] Because the embedded TAPs have different length instruction registers, the chip level TAP includes a flexible length instruction register architecture 120 adapted to accommodate the different length instruction registers 112-118 of the embedded TAPs 104-110. Further, the invention includes selection logic 130 adapted to actively connect only a single embedded TAP to the chip level TAP 102 at a time.

[0021] The inventive flexible length instruction register 120 has, for example in one embodiment, a first instruction register segment 122 having the same length (e.g., 4 bits) as

the shortest embedded TAP instruction register 112, and an additional instruction registers segment (e.g., 2 bit register segment 124) that has an incremental lengths equal to the difference between the previous shorter four bit embedded TAP instruction register 112 and the next largest six bit embedded TAP instruction registers 114, 116, and a third additional instruction register segment (e.g. 4 bit register segment 126) that has an incremental length equal to the difference between the sum of the previous register segments 124 and 122 and the length of embedded TAP instruction register 118. Therefore, when connected to embedded register 118, the invention only actively utilizes the last instruction register segment 128 to shift out (read) the data from the embedded register 118. To the contrary, the invention will utilize both the last and next to last instruction registers segments 128 and 126 to make the flexible length instruction register 120 six bits long, when shifting out data from the six bit embedded registers 114, 116. Similarly, when reading out data from the four bit embedded TAP instruction register 112, the flexible length instruction register 120 will become eight bits in length by engaging the last three instruction register segments 124, 126 and 128. When ac-

cessing the chip level TAP, the flexible length instruction register 120 will become a 12 bit instruction register by engaging all four instruction register segments 122-128.

[0022]   The flexible length instruction register 120 is longer than the longest embedded TAP instruction register. More specifically, the flexible length instruction register 120 has a total of 12 bits divided into separate registers 122-128. The additional bits 128 that make the flexible length instruction register longer than the longest embedded TAP instruction register (e.g., 10 bit register 118) comprises bits 128 that are adapted to choose the effective (active) length of the flexible length instruction register. The selection logic 130 uses the information within the additional bits 128 to identify which embedded TAP will be connected to the chip level TAP 120 and which corresponding registers segments 122-126 will be utilized within the flexible length instruction register 120 to access (shift out) the data from the selected embedded TAP.

[0023]   The integrated circuit chip 100 shown in Figure 1 includes four embedded TAPs 104-110 and three different length instruction registers; however, as would be understood by one ordinarily skilled in the art in light of this disclosure,

any number of embedded TAPs and any number of different length instruction registers could be accommodated with the invention, and the invention is not limited to the specific examples used herein. Further, the selection logic 130 could comprise a wide variety of logic devices as would be understood by one ordinarily skilled in the art. For example, selection logic 130 could include a plurality of multiplexors connected to the instruction registers segments 122–126, wherein the multiplexors could selectively include incremental ones of the additional instruction registers segments to incrementally match the difference in length of the embedded TAP instruction registers and the chip level TAP IR length definition. Thus, the active length of the flexible length instruction register 120 comprises the length of the additional bits 128 combined with selected ones of the additional instruction registers segments 122–126.

[0024] Figures 2 and 3 illustrate a more specific schematic circuit diagram of the invention as it would apply to an integrated circuit chip that included two embedded TAPs 300, 302. More specifically, Figure 2 illustrates the instruction shift registers 200–204 that are found within the first embedded TAP 300, second embedded TAP 302, and the

chip level TAP 304, respectively, that are shown in Figure 3.

[0025] A given embedded TAP instruction register 200, 202 "maps" onto the chip-level instruction register 310-314 starting at the most significant bit (MSB) such as bit 9 of the IR definition and proceeding downwards as shown in Figure 2. Figure 2 illustrates two embedded TAP IRs 200, 202 that are 5 and 8 bits in length, respectively, for embedded TAP #1 300 and embedded TAP #2 302. As shown in Figure 3, the chip-level TAP IR is 10 bits in length (L=K+D) where K is equal to the total of the individual shift registers 310, 312 and D is equal to the number of additional control bits 314. More specifically, the chip-level TAP instruction register is designed with a length $L = K+D$, where $K >=$ (length of longest instruction register, or string of instruction registers if serially connected, among TAPS in embedded IP blocks) and $2^D > N$, where N= (# of TAPs in embedded IP blocks). The D low-order bits of the instruction register will be used for selecting access to the TAP within one of the N IP blocks or for selecting a chip-level instruction.

[0026] Figure 3 shows that when a TAP controller of embedded IP blocks is accessed by the decoded D low-order bits 314

of the instruction register (bits[1:0]), and the SHIFT-IR state is entered by the chip-level TAP controller 304, the chip-level TAP IR is instructed (by the TAP logic unit 322) to connect the embedded TAP test data output (TDO) signal in place of the instruction register bit corresponding to the length of the chip-level IR, less the length of the selected embedded TAP IR. For embedded TAP #1, as defined above, this is bit 5 (10-5), IR5 shown in Figure 2; for embedded TAP #2, this is bit 2 (10-8), IR2 shown in Figure 2.

[0027] With respect to the additional structure shown in Figure 3, the TAP logic unit 322 can receive a number of different inputs including a test clock signal (TCK), a test data input (TDI), the low order bits (IR1, IR0) that identify which, if any, embedded TAP controller will be accessed, a test mode select signal (TMS) that controls test operations, and a test reset signal (TRST). Using these inputs, the TAP logic controller 322 controls AND gates 318, which in turn control multiplexors 316 to selectively utilize none, one, or both of the shift register 310, 312. The same control signals that are sent to AND gates 318 are also provided to the OR gates 320 to enable or disable the embedded TAP controllers 300, 302 so that no more than one of the

embedded TAP controllers is providing data to the chip-level TAP at a time.

[0028] The structure shown in Figure 3 allows the TAP controller, in the selected embedded IP block, to track synchronously, state for state, with the chip-level TAP controller logical state. Since the selected embedded TAP controller and the chip-level TAP controller will be running synchronously, when a SHIFT-IR state is entered by the chip-level TAP logic 322, it is also entered in the selected embedded TAP controller. Under these conditions the IR shift out of the chip-level TAP controller will match the "mapped" definition shown in Figure 2. As shown in Figure 3, with embedded TAP #1 300 selected, the first 5 bits will come from the chip-level TAP IR segments 312, 314 and the last 5 bits will come from the embedded TAP IR 300 rather then from register segment 310. In a similar manner, if TAP #2 302 is being accessed, its eight bits of data will be preceded by the two bits from the chip-level TAP instruction register segment 314.

[0029] While the invention has been described in terms of selecting between two TAPs of differing instruction register lengths, those skilled in the art will recognize that the invention also applies equally to a single embedded tap or

to multiple serial strings of embedded TAPs, as shown in Figure 4. The length of the instruction register of TAP string #1 is the sum of the lengths of instruction registers in embedded TAPs 1a 1n 400-402.

[0030] Therefore, as shown above, one benefit of the invention is that the flexible length instruction register appears as a fixed length instruction register to users connecting to the chip level TAP. Therefore, the invention allows IEEE1149.1 compliant access (reading) of embedded JTAG TAP controller instruction register (IR) contents, contained in IP blocks on ASIC chips, while using a constant length chip level instruction register definition for all IR accesses through the chip level TAP. More specifically, the invention allows positional bit replacement of the chip level TAP IR data with embedded TAP IR data. The inventive architecture allows for a single IR length definition to represent and access all embedded and chip level TAP instruction registers.

[0031] In the invention, there is no need for chip-level Compliance-Enable (CE) pins (the invention maintains compliance to the Standard while solving a problem not addressed by the Standard). The invention does not add to board-test complexity (control/access to CE pins). Further, in the in-

vention, no special treatment is needed at test time or during functional operation. The invention does not require multiple BSDL files to account for different instruction register lengths. The invention eliminates need for extra I/O dedicated to test.

[0032] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.